# DATA SHEET

# TDA1515BQ
## 24 W BTL or 2 x 12 W stereo car radio power amplifier

Product specification
File under Integrated Circuits, IC01

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Philips Semiconductors

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# 24 W BTL or 2 x 12 W stereo car radio power amplifier

# TDA1515BQ

The TDA1515BQ is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage $V_P$ = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 × 12 W into 2 Ω or 2 × 7 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability.

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to $V_P$ = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe.

# 24 W BTL or 2 x 12 W stereo car radio power amplifier

# TDA1515BQ

## QUICK REFERENCE DATA

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range (operating) | $V_P$ | | | 6 to 18 | V |
| Supply voltage (non-operating) | $V_P$ | max. | | 28 | V |
| Supply voltage (non-operating; load dump protection) | $V_P$ | max. | | 45 | V |
| Repetitive peak output current | $I_{ORM}$ | max. | | 4 | A |
| Total quiescent current | $I_{tot}$ | typ. | | 75 | mA |
| Stand-by current | $I_{sb}$ | typ. | | 1 | μA |
| Switch-on current | $I_{so}$ | < | | 100 | μA |
| Input impedance | $\lvert Z_i \rvert$ | > | | 1 | MΩ |
| **Bridge tied load application (BTL)** | $V_P$ | = | 14,4 | 13,2 | V |
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | | |
| **$d_{tot}$ = 0,5%** | $P_o$ | typ. | 18 | 15 | W |
| $d_{tot}$ = 10% | $P_o$ | typ. | 24 | 20 | W |
| Supply voltage ripple rejection; $R_S$ = 0 Ω; f = 100 Hz | RR | typ. | 50 | 50 | dB |
| D.C. output offset voltage between the outputs | $\lvert \Delta V_{5-9} \rvert$ | < | 50 | 50 | mV |
| **Stereo application** | | | | | |
| Output power at $d_{tot}$ = 10% (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 7 | 6 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 12 | 10 | W |
| Output power at **$d_{tot}$ = 0,5%** (with bootstrap) | | | | | |
| $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 | 4,5 | W |
| $R_L$ = 2 Ω | $P_o$ | typ. | 9 | 7,5 | W |
| Channel separation | α | > | 40 | 40 | dB |
| Noise output voltage; $R_S$ = 10 kΩ; according to IEC curve-A | $V_n$ | typ. | 0,2 | 0,2 | mV |

## PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C); SOT141-6; 1996 July 19.

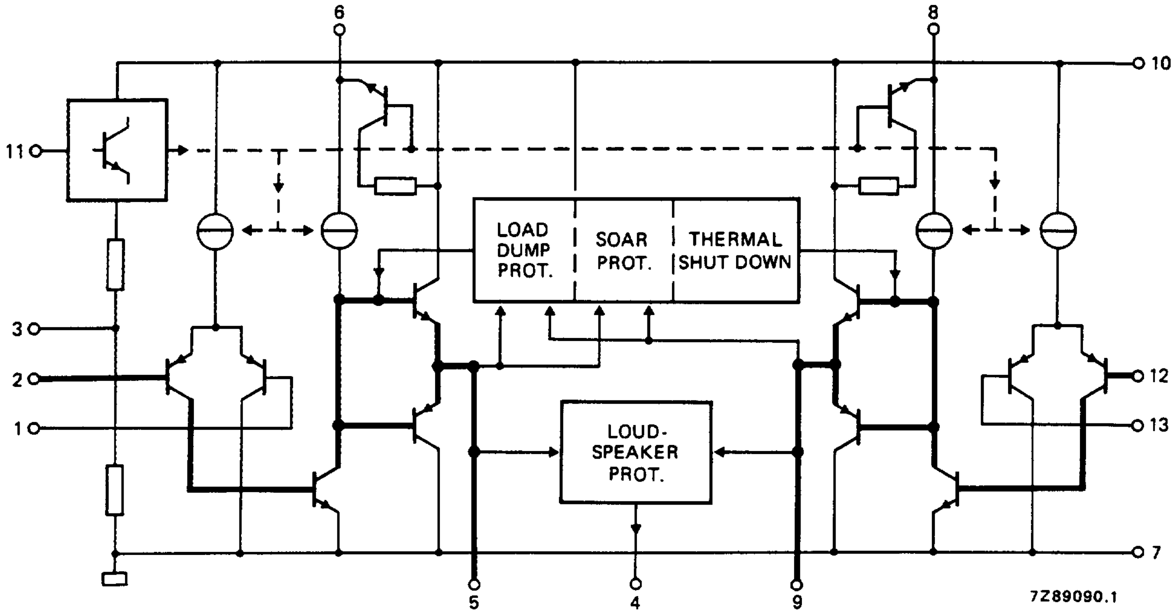



Fig.1 Internal block diagram; the heavy lines indicate the signal paths.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|---|---|---|---|
| Supply voltage; operating (pin 10) | $V_P$ | max. | 18 V |
| Supply voltage; non-operating | $V_P$ | max. | 28 V |
| Supply voltage; during 50 ms (load dump protection) | $V_P$ | max. | 45 V |
| Peak output current | $I_{OM}$ | max. | 6 A |
| Total power dissipation | see derating curve Fig.2 | | |
| Storage temperature range | $T_{stg}$ | | –55 to + 150 °C |
| Crystal temperature | $T_c$ | max. | 150 °C |
| A.C. and d.c. short-circuit safe voltage | | max. | 18 V |
| Reverse polarity | | max. | 10 V |

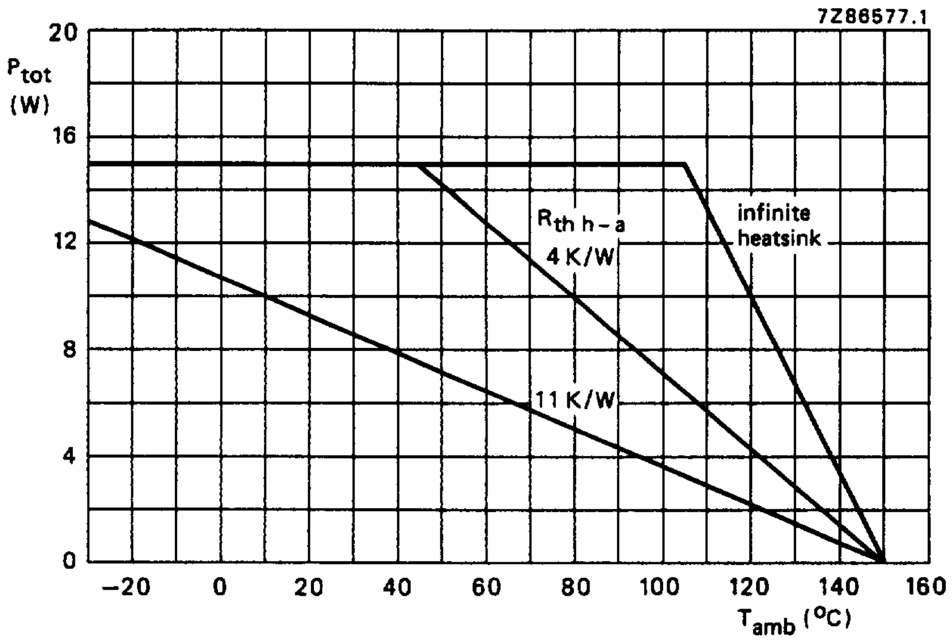



Fig.2 Power derating curves.

**HEATSINK DESIGN EXAMPLE**

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 × 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

$T_{amb}$ = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} = -3 = 4\ \text{K/W}$$

2 × 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

$T_{amb}$ = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} = -3 = 11\ \text{K/W}$$

## D.C. CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Supply voltage range (pin 10) | | $V_P$ | | 6 to 18 | V |
| Repetitive peak output current | | $I_{ORM}$ | < | 4 | A |
| Total quiescent current | | $I_{tot}$ | typ. | 75 | mA |
| Switching level 11: | OFF | $V_{11}$ | < | 1,8 | V |
| | ON | $V_{11}$ | > | 3 | V |
| Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11}$ < 1,8 V) | | $\lvert Z_{OFF} \rvert$ | > | 100 | kΩ |
| Stand-by current at $V_{11}$ = 0 to 0,8 V | | $I_{sb}$ | typ. | 1 | µA |
| | | | < | 100 | µA |
| Switch-on current (pin 11) at $V_{11} \leq V_{10}$ (note 1) | | $I_{so}$ | typ. | 10 | µA |
| | | | < | 100 | µA |

## A.C. CHARACTERISTICS

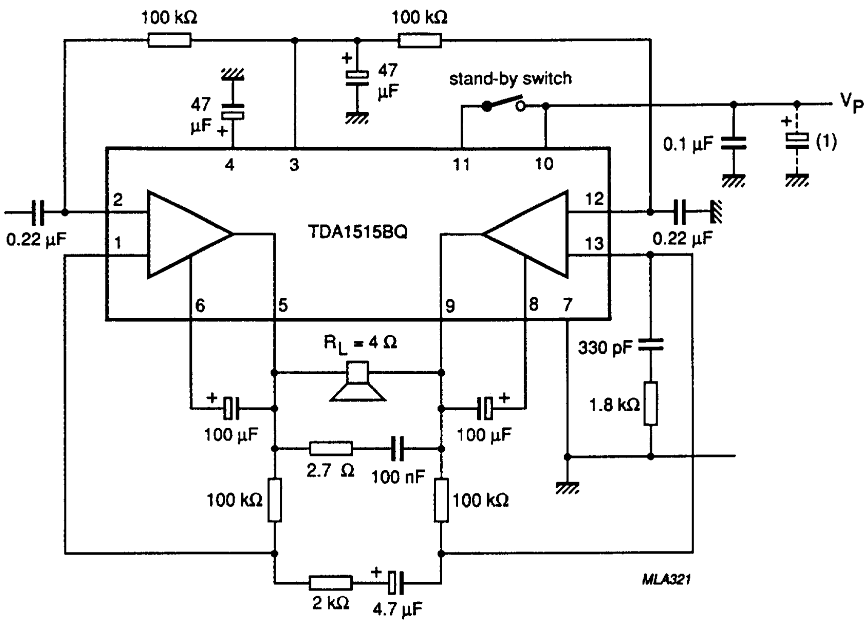
$T_{amb}$ = 25 °C; $V_P$ = 14,4 V; f = 1 kHz; unless otherwise specified

| | | | | |
|---|---|---|---|---|
| **Bridge tied load application (BTL); see Fig.3** | | | | |
| Output power at $R_L$ = 4 Ω (with bootstrap) | | | | |
| $V_P$ = 14,4 V; **$d_{tot}$ = 0,5%** | $P_o$ | > | 15,5 | W |
| | | typ. | 18 | W |
| $V_P$ = 14,4 V; $d_{tot}$ = 10% | $P_o$ | > | 20 | W |
| | | typ. | 24 | W |
| $V_P$ = 13,2 V; **$d_{tot}$ = 0,5%** | $P_o$ | typ. | 15 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 10% | $P_o$ | typ. | 20 | W |
| Open loop voltage gain | $G_o$ | typ. | 75 | dB |
| Closed loop voltage gain (note 2) | $G_c$ | typ. | 40 (± 0,5) | dB |
| Output power without bootstrap (note 9) | | | | |
| $V_P$ = 14,4 V; $d_{tot}$ = 10% | $P_o$ | typ. | 15 | W |
| $V_P$ = 14,4 V; $d_{tot}$ = 0,5% | $P_o$ | typ. | 12 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 10% | $P_o$ | typ. | 12 | W |
| $V_P$ = 13,2 V; $d_{tot}$ = 0,5% | $P_o$ | typ. | 9 | W |
| Frequency response at –3 dB (note 3) | B | | 20 Hz to min. 20 | kHz |
| Input impedance (note 4) | $\lvert Z_i \rvert$ | > | 1 | MΩ |
| Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,2 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,35 | mV |
| | | < | 0,8 | mV |
| $R_S$ = 10 kΩ; according to IEC 179 curve A | $V_n$ | typ. | 0,25 | mV |
| Supply voltage ripple rejection (note 5) | | | | |
| f = 100 Hz | RR | > | 42 | dB |
| | | typ. | 50 | dB |

| | | | | |
|---|---|---|---|---|
| D.C. output offset voltage between the outputs | $\lvert\Delta V_{5\text{-}9}\rvert$ | < | 50 | mV |
| | | typ. | 2 | mV |
| Loudspeaker protection (all conditions) | | | | |
| maximum d.c. voltage (across the load) | $\lvert\Delta V_{5\text{-}9}\rvert$ | < | 1 | V |
| Power bandwidth; –1 dB; **$d_{tot}$ = 0,5%** | B | | 30 Hz to 40 | kHz |
| **Stereo application; see Fig.4** | | | | |
| Output power at $d_{tot}$ = 10%; with bootstrap (note 6) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | > | 6 | W |
| | | typ. | 7 | W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | > | 10 | W |
| | | typ. | 12 | W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 6 | W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 10 | W |
| Output power at **$d_{tot}$ = 0,5%**; with bootstrap (note 6) | | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω | $P_o$ | typ. | 5,5 | W |
| $V_P$ = 14,4 V; $R_L$ = 2 Ω | $P_o$ | typ. | 9 | W |
| $V_P$ = 13,2 V; $R_L$ = 4 Ω | $P_o$ | typ. | 4,5 | W |
| $V_P$ = 13,2 V; $R_L$ = 2 Ω | $P_o$ | typ. | 7,5 | W |
| Output power at $d_{tot}$ = 10%; without bootstrap | | | | |
| $V_P$ = 14,4 V; $R_L$ = 4 Ω (notes 6, 8 and 9) | $P_o$ | typ. | 6 | W |
| Frequency response at –3 dB (note 3) | B | | 40 Hz to min. 20 | kHz |
| Supply voltage ripple rejection (note 5) | RR | typ. | 50 | dB |
| Channel separation; $R_S$ = 10 kΩ; f = 1 kHz | α | > | 40 | dB |
| | | typ. | 50 | dB |
| Closed loop voltage gain (note 7) | $G_c$ | typ. | 40 | dB |
| Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz | | | | |
| $R_S$ = 0 Ω | $V_{n(rms)}$ | typ. | 0,15 | mV |
| $R_S$ = 10 kΩ | $V_{n(rms)}$ | typ. | 0,25 | mV |
| $R_S$ = 10 kΩ; according to IEC 179 curve A | $V_n$ | typ. | 0,2 | mV |

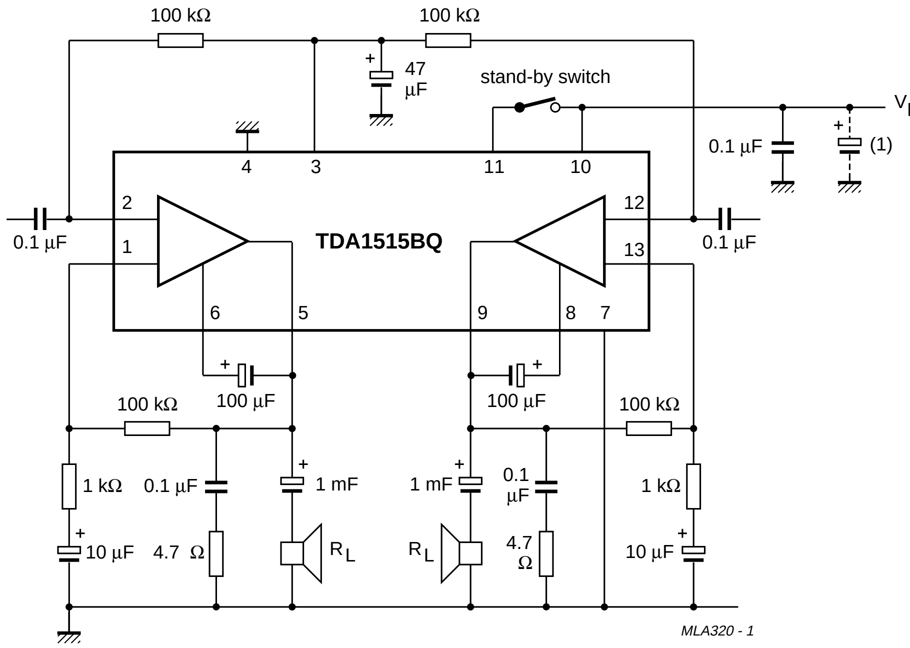
**Notes**

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig.3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.




(1) Belongs to power supply.

Fig.3 Test/application circuit bridge tied load (BTL).

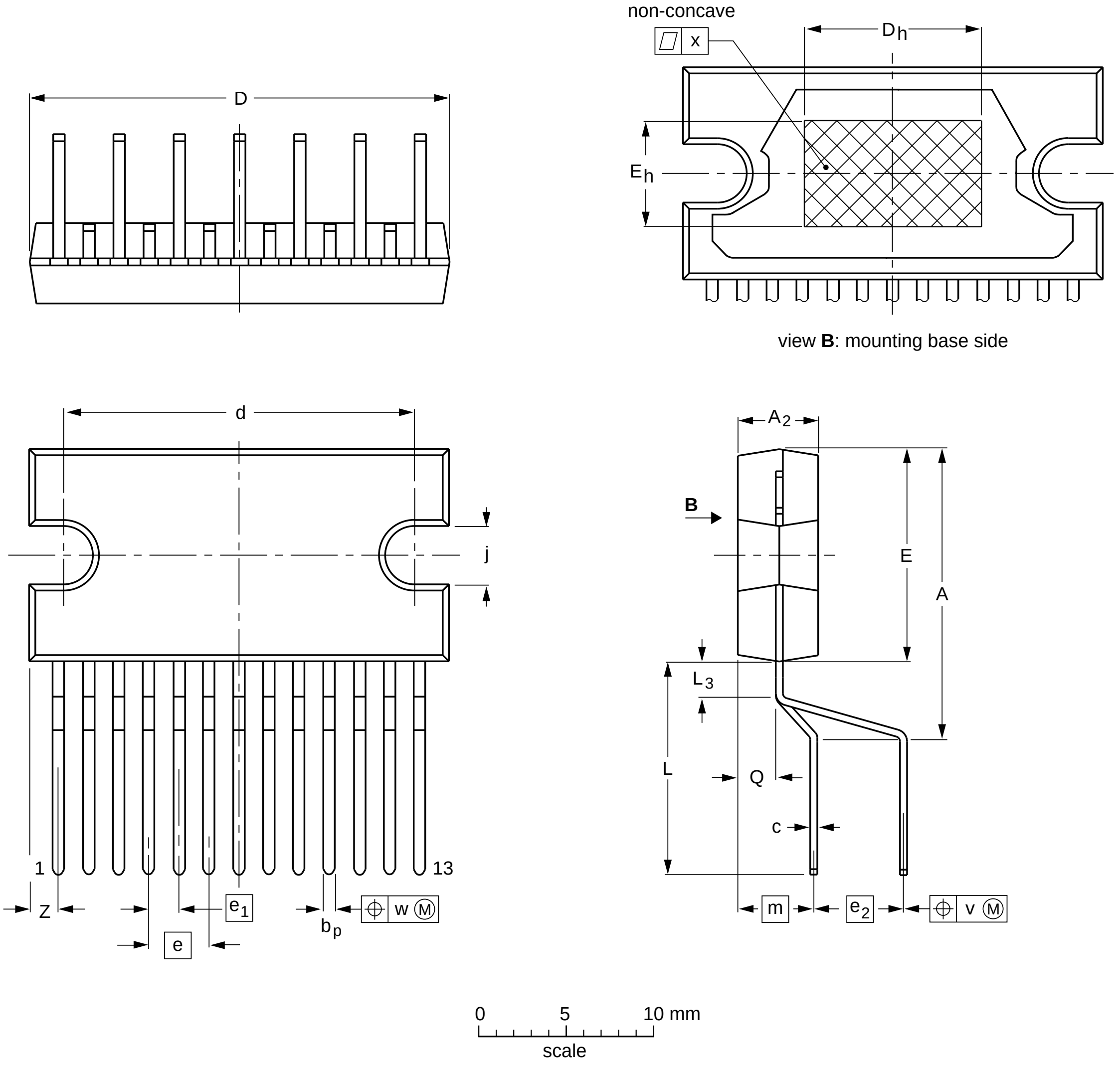



(1) Belongs to power supply.

Fig.4 Test/application circuit stereo.

## PACKAGE OUTLINE

**DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)** **SOT141-6**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_2$ | $b_p$ | c | $D^{(1)}$ | d | $D_h$ | $E^{(1)}$ | e | $e_1$ | $e_2$ | $E_h$ | j | L | $L_3$ | m | Q | v | w | x | $Z^{(1)}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 17.0<br>15.5 | 4.6<br>4.2 | 0.75<br>0.60 | 0.48<br>0.38 | 24.0<br>23.6 | 20.0<br>19.6 | 10 | 12.2<br>11.8 | 3.4 | 1.7 | 5.08 | 6 | 3.4<br>3.1 | 12.4<br>11.0 | 2.4<br>1.6 | 4.3 | 2.1<br>1.8 | 0.8 | 0.25 | 0.03 | 2.00<br>1.45 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT141-6 | | | | | | ~~92-11-17~~<br>95-03-11 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.